Spread Spectrum Series, Part Two

Correlators are an important basic building block in CDMA designs. Correlators are used in signal acquisition, tracking and demodulation circuits and occupy a substantial amount of system resources. The correlator design is often the determining factor in how fast a system can acquire a signal, tolerate interference and the magnitude of silicon required; optimizing correlators for a specific CDMA design is crucial.

This article considers the two basic “correlator” types. Figure 1 is a correlator and figure 2 is a matched filter. The terms correlator and matched filter are often used interchangeably. Correlators are well understood and covered in many texts; presented here are correlators found in product designs, their output and some performance tradeoffs and optimizations that must be made when a correlator is designed for both a specific standard and the technology that will be used to implement the system.

**Correlator and Matched Filter Review**

A Correlator, figure 1, can be easily described and understood as pattern matcher. The signal $r(t)$ is typically a demodulated baseband signal from the RF, and $p_n(t)$ is a copy of the spreading code. If $r(t)$ and $p_n(t)$ are considered as bipolar signals, then when the two are identical and in phase an output will appear at $z(T)$ when the sampler (switch) is closed. If the signals on average match only half of the time, a 0 is sampled at $z(T)$ when the switch is closed. This is a simple example of correlation and processing gain that makes CDMA work. The desired signal, the one that is to be demodulated, matches the $p_n$ code and produces a response. Noise, including other signals or users, matches the $p_n$ code half the time and does not produce an output. It has been assumed that $r(t)$ and $p_n(t)$ are synchronized; practical circuits that acquire and maintain synchronization will be examined in other articles in this series.

Most technical texts describe $r(t)$ as an analog signal or a one-bit digital signal. In most current CDMA digital receivers, $r(t)$ is a composite of many signals that have been quantized by a multi-bit A/D converter. If the circuit does not saturate, the components of $r(t)$ that match the $p_n$ will accumulate and components not matching $p_n(t)$ will tend to average to zero.

A matched filter correlator appears in figure 2. If the sampler is synchronized to close when $r(t)$ is aligned to $p_n(t)$, the output is identical to the correlator. The number of stages ($m$) is typically equal to the length of the $p_n$ code, but it may also be a fraction of the code length.

![Figure 1: Correlator Type Receiver](image)
Correlator and Matched Filter Circuits

A correlator circuit schematic appears in figure 3. For this implementation, the A/D was centered about its mid-range (80H). The input is from an 8-bit A/D converter that is then multiplied, or compared, to the current state of pn(t). A full scale high (FFH) when multiplied by a 1 produces a value of 80. A full-scale low (00H) when multiplied by a 0 also produces a value of 80. The output of the multiplier is a 1’s compliment number.

It is illustrative and convenient to consider the output of the multiplier as a 1’s compliment fraction that represents the percentage of match between the received signal r(t) and the current state of the spreading code pn(t). A large negative value indicates a large match, and a large positive indicates a large match between r(t) and the inverse of pn(t). A small positive or negative value indicates nearly no match. Remember, the received signal r(t) is typically composed of many signals and noise. The output of the multiplier is then integrated with a digital adder and register that form an accumulator. The circuit is initialized via the multiplexer, mux.

Figure 4 is a matched filter used in an 802.11 design for correlating a Barker spreading code. The output of this circuit appears in figure 5. The output is used to measure signal quality and multipath. The sampling switch of the matched filter, figure 2, is sampled every cycle. Every clock cycle outputs a value representative of the correlation between the received signal and phase shifts of the spreading code. This circuit is much larger that the correlator, but is advantageous when searching for signals.

Figure 6 is the output of a matched filter type correlator optimized for the IS-95 standard, the Xilinx FPGA architecture and speed. The magnitude of pilot pn signals versus time of arrival is plotted. Pilot pn codes may originate from different Base Stations or may be due to multipath. All pn phases (32,768) for IS-95 are calculated in 27mSec. Figure 7 shows how two distinct pilot pn signals, formed via multipath, correlate with the IS-95 pn code at the receiver.
Barker code: 1011 0111 000
Input Data
PN Code
1-Bit Multiply
Adder
Pipeline Register
Adder
Shift (scale)
Pipeline Register
Adder
Adder
Conversion to Sign and Magnitude

Figure 3: Correlator Circuit

Figure 4: Matched Filter Circuit
figure 5: Output of the 802.11 Barker Matched Filter shown in figure 4. The magnitude of Barker codes received versus time of arrival is plotted.

Figure 6: The output of matched filter type correlator optimized for the IS-95 standard, the Xilinx® FPGA architecture and speed is shown here. The magnitude of pilot pn signals versus time of arrival is plotted. Pilot pn codes may originate from different Base Stations or may be due to multipath. All pn phases (32,768) for IS-95 are calculated in 27mSec.
Figure 7: Two distinct pilot pn signals, formed via multipath, correlate with the IS-95 pn code at the receiver.

**Math and Number Representation**
The correlator and matched filter cited above use 1’s compliment math. This is convenient and usually results in a small correlator design. The output of the correlator connects to a variety of other circuits that may be simplified if numbers are represented differently. Multipliers, for example, are simpler if they multiply sign and magnitudes. The output of the correlator should accommodate the type of circuit that it will be connected to. The matched filter shown in figure 4 converts its output to sign and magnitude.

**Number of Bits and Compressing**
Since the received signal contains the signal to be demodulated and interference, it is important quantize the composite signal with enough bits so that it does not underflow. Since interference tends not to accumulate over the integration time, all of the bits output by the correlator may not be significant. The large number of bits at the input of a correlator, especially when combined with a long integration time, result in a correlator with large adders and a large number of bits at its output. The output of the correlator often connects to other circuits that contain multipliers or comparitors and produce even more bits and circuit size.

Figure 8 depicts some typical compressor circuits. Figure 9 shows how they can be used to reduce the number of bits output by a correlator. Simulation with the system pn code, maximum and minimum number of users on the same channel, noise and channel fading characteristics must be simulated and tested to insure that the correlator does not overflow and compromise performance.
Figure 8: Typical Compressors

a. Transfer function of a limiter and its symbol.

b. Transfer function of a scaler and its symbol.

c. Transfer function of a log compressor and its symbol.

Figure 9: Typical schemes to reduce the number of bits output by a correlator.

a. Input limited (may be unintentional a saturated A/D)

b. Scaled output

c. Limited output

d. Log compressed output

e. Integrator with limited feedback
Architecture, Speed, Size and Technology
Correlators are implemented in both hardware and in software designed for Digital Signal Processors (DSPs). Real-time correlation that is required for continuous demodulation and tracking usually require dedicated correlators in hardware. It does depend on the particular system and the designer, but high pn code rates and the cost of high performance DSPs make dedicated hardware in FPGA or ASIC a good choice.

The relatively small circuit size of correlator type architecture is the best choice for demodulator circuits because the pn code is already phase aligned to the received signal. A matched filter architecture is desirable for the fast signal searching applications as shown in figures 5 and 6. Multiple correlators that run in parallel with different phases of the pn code may achieve the same performance in a similar circuit size. The regular pattern of the matched filter shown in figure 4, low signal fanout and pipelined architecture results in a much simpler placement in FPGA or ASIC.

The correlator whose output appears in figure 5 was realized in a Xilinx® FPGA. The circuit size, compared to a standard correlator architecture, was reduced by a factor of 8 with careful optimization for the specific resources found in a Xilinx® FPGA.

Conclusion
It is critical to optimize the correlator design for both the specific system and for the technology used to implement the design. Correlators will impact the system performance and determine the magnitude of hardware needed for the system. Future articles in this series will present practical circuits and concepts for signal acquisition, signal tracking and data demodulation. The correlator is the basis of these CDMA circuits.

Footnotes:

Figure 5 displays Berkeley’s newest WLAN receiver the Grasshopper.

Figure 6 & 7 display output from Berkeley’s high-end PN scanner the Super Eagle.